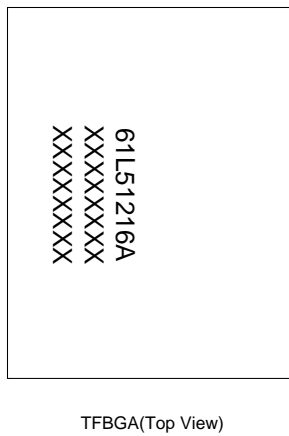
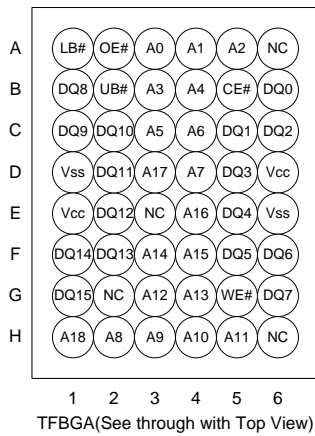
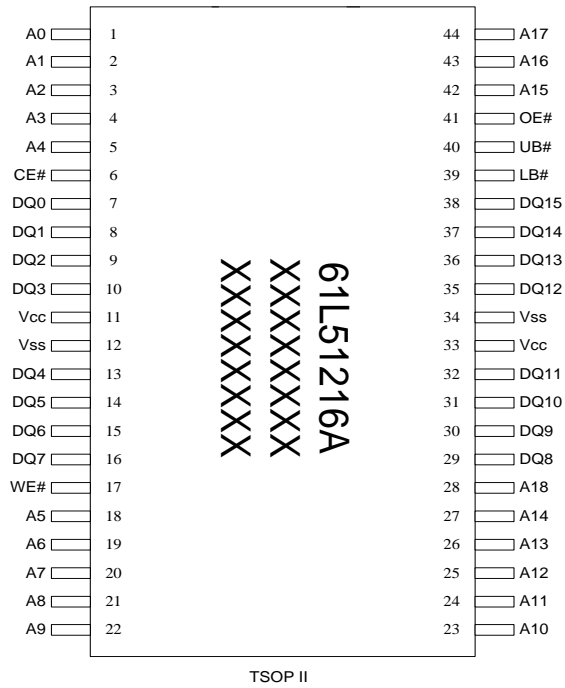


REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.a	Initial Issued	Mar.18.2019

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{CC} relative to V _{SS}	V _{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V _{SS}	V _{T2}	-0.5 to V _{CC} +0.5	V
Operating Temperature	T _A	-40 to 85(I grade)	°C
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
						DQ0 - DQ7	DQ8 - DQ15	
Standby	H	X	X	X	X	High-Z	High-Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	X	X	High-Z	High-Z	I _{CC} , I _{CC1}
	L	X	X	H	H	High-Z	High-Z	
Read	L	L	H	L	H	D _{OUT}	High-Z	I _{CC} , I _{CC1}
	L	L	H	H	L	High-Z	D _{OUT}	
	L	L	H	L	L	D _{OUT}	D _{OUT}	
Write	L	X	L	L	H	D _{IN}	High-Z	I _{CC} , I _{CC1}
	L	X	L	H	L	High-Z	D _{IN}	
	L	X	L	L	L	D _{IN}	D _{IN}	

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ⁴	MAX.	UNIT	
Supply Voltage	V _{CC}		-8	3.0	3.3	3.6	V
			-10	2.7	3.3	3.6	V
Input High Voltage	V _{IH} ¹		2.2	-	V _{CC} +0.3	V	
Input Low Voltage	V _{IL} ²		- 0.3	-	0.8	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	- 1	-	1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	- 1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -4mA	2.4	-	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 8mA	-	-	0.4	V	
Average Operating Power Supply Current	I _{CC}	Cycle time = MIN. CE# = V _{IL} , I _{I/O} = 0mA, Others at V _{IL} or V _{IH}	-8	-	110	140	mA
			-10	-	100	130	mA
	I _{CC1}	CE# ≤ 0.2, Others at 0.2V or V _{CC} -0.2V I _{I/O} = 0mA; f=max	-8	-	90	120	mA
			-10	-	80	110	mA
Standby Power Supply Current	I _{SB}	CE# = V _{IH} , Others at V _{IL} or V _{IH}	-	-	40	mA	
	I _{SB1}	CE# ≥ V _{CC} - 0.2V, Others at 0.2V or V _{CC} - 0.2V	-	3	25	mA	

Notes:

- V_{IH(max)} = V_{CC} + 2.0V for pulse width less than 6ns.
- V_{IL(min)} = V_{SS} - 2.0V for pulse width less than 6ns.
- Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
- Typical values are included for reference only and are not guaranteed or tested.

Typical values are measured at V_{CC} = V_{CC(TYP)} and T_A = 25°C

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C _{IN}	-	8	pF
Input/Output Capacitance	C _{I/O}	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Speed	8/10ns
Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -4mA/8mA

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	61L51216A-8		61L51216A-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	8	-	10	-	ns
Address Access Time	t _{AA}	-	8	-	10	ns
Chip Enable Access Time	t _{ACE}	-	8	-	10	ns
Output Enable Access Time	t _{OE}	-	4.5	-	4.5	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	2	-	2	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	0	-	0	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	3	-	4	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	3	-	4	ns
Output Hold from Address Change	t _{OH}	2	-	2	-	ns
LB#, UB# Access Time	t _{BA}	-	4.5	-	4.5	ns
LB#, UB# to High-Z Output	t _{BHZ} *	-	3	-	4	ns
LB#, UB# to Low-Z Output	t _{BLZ} *	0	-	0	-	ns

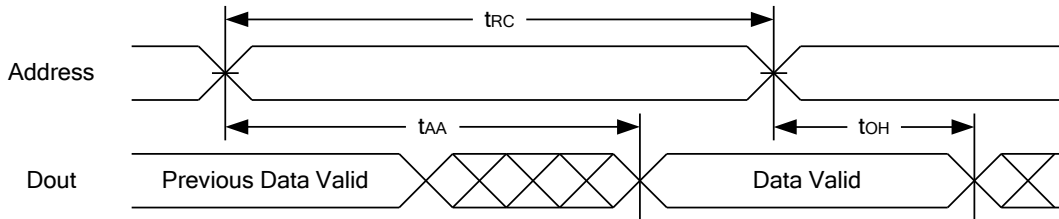
(2) WRITE CYCLE

PARAMETER	SYM.	61L51216A-8		61L51216A-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	8	-	10	-	ns
Address Valid to End of Write	t _{AW}	6.5	-	8	-	ns
Chip Enable to End of Write	t _{CW}	6.5	-	8	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	ns
Write Pulse Width	t _{WP}	6.5	-	8	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	5	-	6	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	2	-	2	-	ns
Write to Output in High-Z	t _{WHZ} *	-	3	-	4	ns
LB#, UB# Valid to End of Write	t _{BW}	6.5	-	8	-	ns

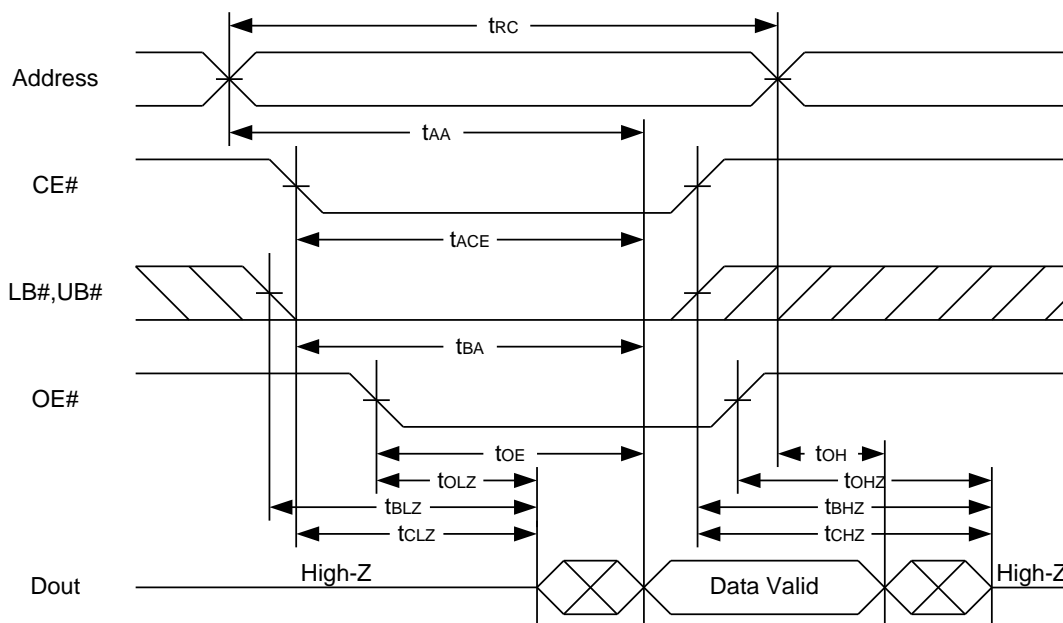
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



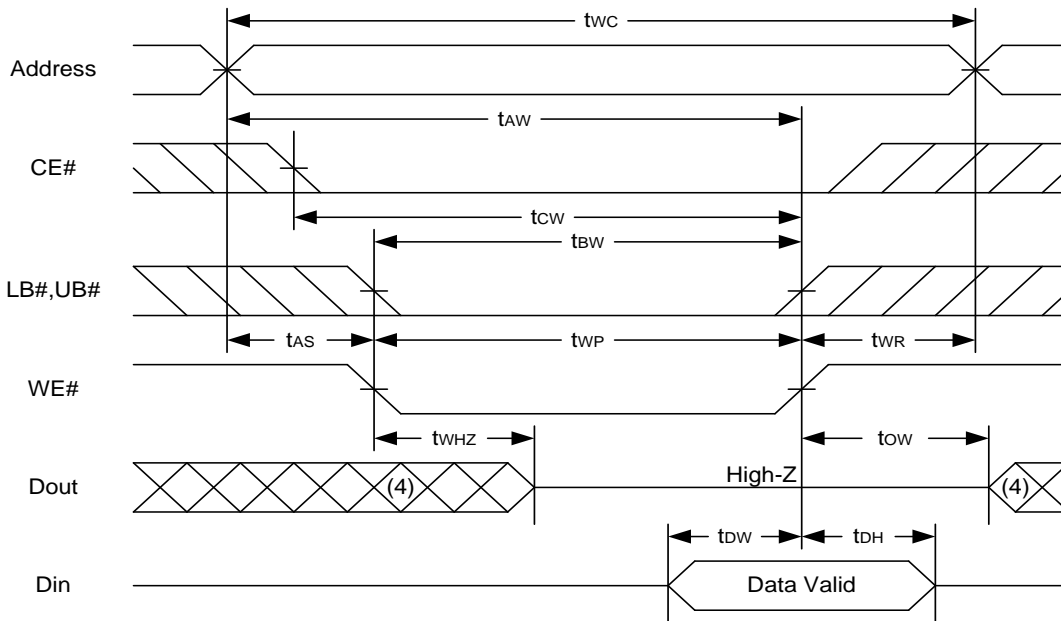
READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)



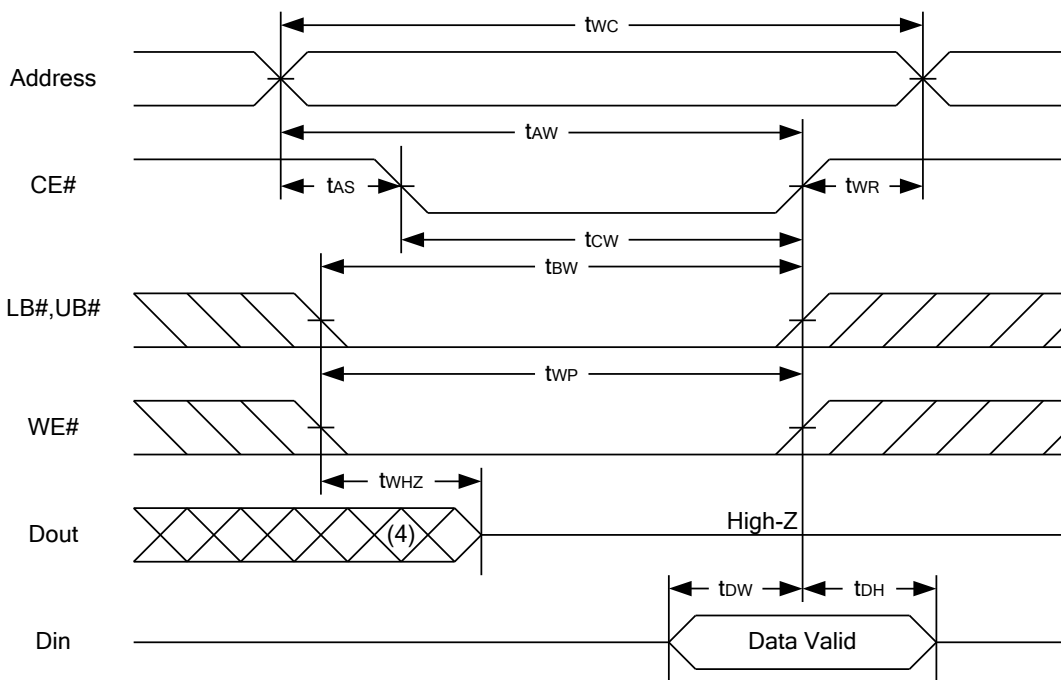
Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{BLZ} , t_{OLZ} , t_{CHZ} , t_{BHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ} , t_{OHZ} is less than t_{OLZ} .

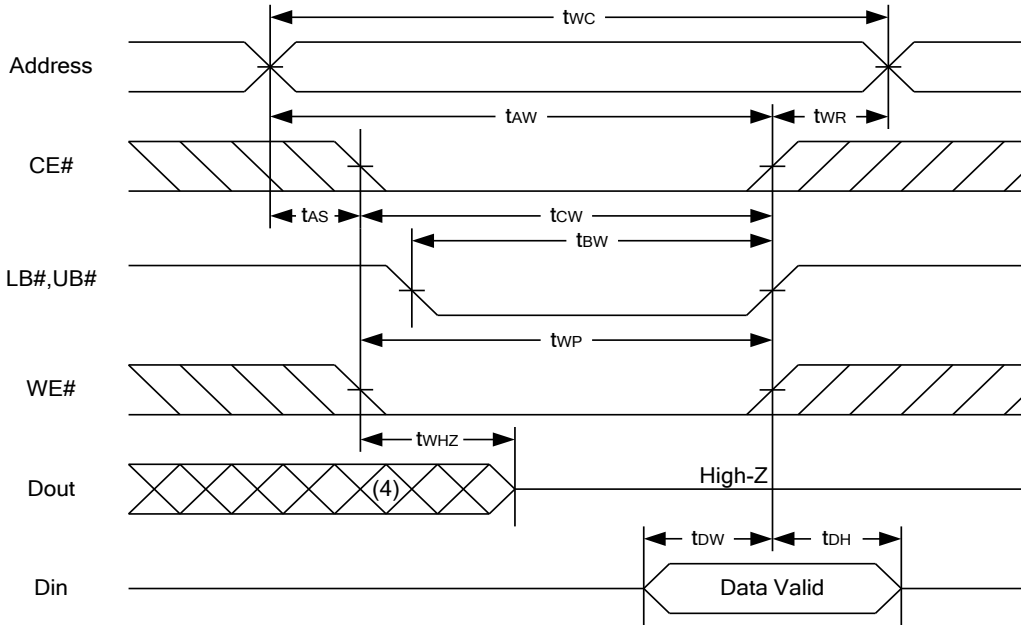
WRITE CYCLE 1 (WE# Controlled) (1,2,4,5)



WRITE CYCLE 2 (CE# Controlled) (1,4,5)



WRITE CYCLE 3 (LB#,UB# Controlled) (1,4,5)



Notes :

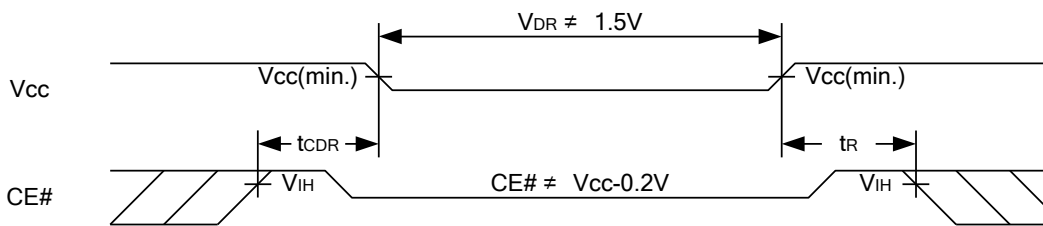
1. A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
2. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
5. t_{OW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V	1.5	-	3.6	V
Data Retention Current	I _{DR}	V _{CC} = 1.5V, CE# ≥ V _{CC} - 0.2V; Other pin is at 0.2V or V _{CC} -0.2V	-	3	25	mA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC} *	-	-	ns

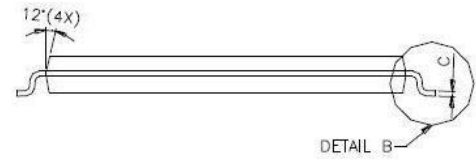
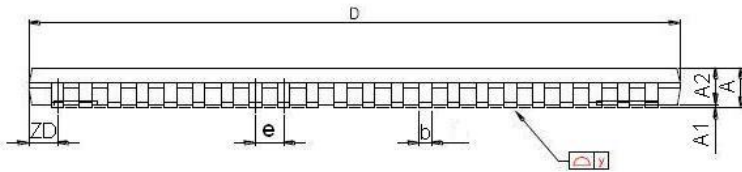
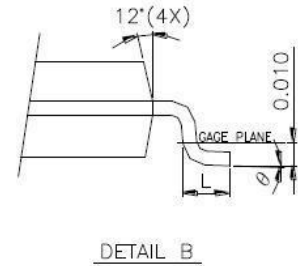
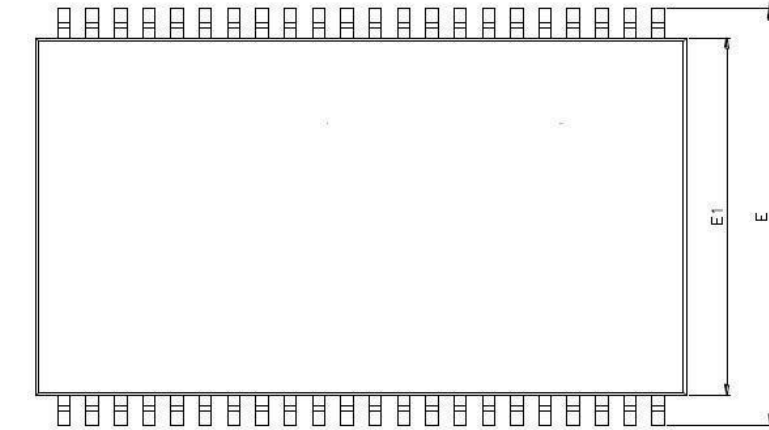
t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM



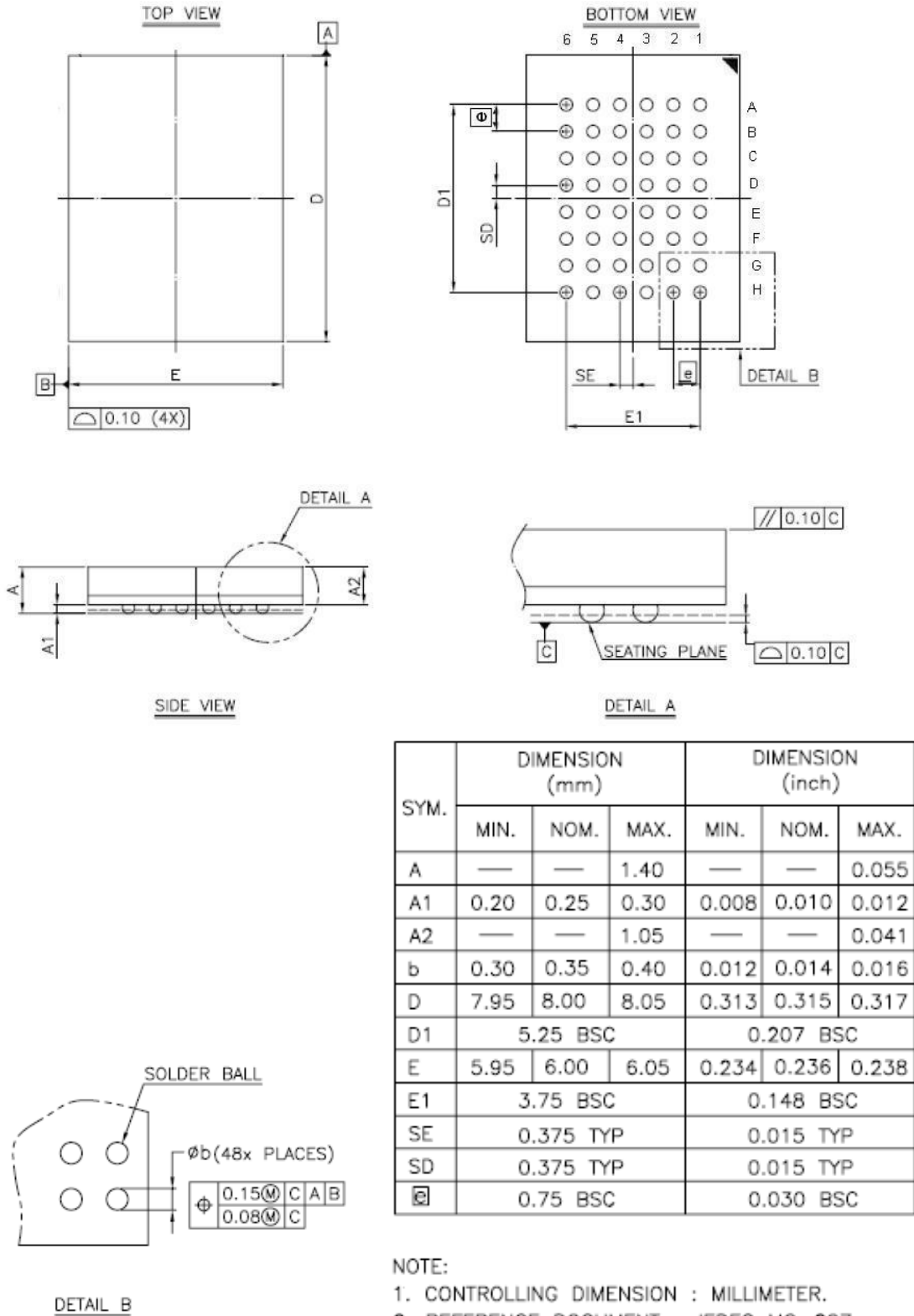
PACKAGE OUTLINE DIMENSION

44-pin 400mil TSOP II Package Outline Dimension



SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°

48-ball 6mm x 8mm TFBGA Package Outline Dimension



ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Temperature Range(°C)	Packing Type	Item No.
44-pin (400mil) TSOP II	8	0°C~70°C	Tray	61L51216AML-8
			Tape Reel	61L51216AML-8T
		-40°C~85°C	Tray	61L51216AML-8I
			Tape Reel	61L51216AML-8IT
	10	0°C~70°C	Tray	61L51216AML-10
			Tape Reel	61L51216AML-10T
		-40°C~85°C	Tray	61L51216AML-10I
			Tape Reel	61L51216AML-10IT

ORDERING INFORMATION

Package Type	Access Time (Speed)(ns)	Temperature Range(°C)	Packing Type	Item No.
48-ball (6mm x 8mm) TFBGA	8	0°C~70°C	Tray	61L51216AGL-8
			Tape Reel	61L51216AGL-8T
		-40°C~85°C	Tray	61L51216AGL-8I
			Tape Reel	61L51216AGL-8IT
	10	0°C~70°C	Tray	61L51216AGL-10
			Tape Reel	61L51216AGL-10T
		-40°C~85°C	Tray	61L51216AGL-10I
			Tape Reel	61L51216AGL-10IT

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